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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,672	08/28/2001	Toshiyuki Hirota	WN-2345	4866

466 7590 10/25/2002

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EXAMINER
LUU, THANH X

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 10/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/939,672	Applicant(s) HIROTA, TOSHIYUKI	
	Examiner Thanh X Luu	Art Unit 2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: communication path "203" of Figure 4, as mentioned on page 9. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 1, 8 and 9 are objected to because of the following informalities:

In claim 1, "the elements" lacks proper antecedent basis because Applicant uses the terms "the elements" and "the processing elements" to refer to the same limitation. Examiner recommends using consistent terminology.

In claim 8, "the light" lacks proper antecedent basis. Further, Examiner believes "each of the processing element" should be –each of the processing elements-- and "between the processing element" should be –between the processing elements--.

In claim 9, last line, Examiner believes "connects the semiconductor chips each other" should be –connects the semiconductor chips to each other--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1-3, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Pocholle et al. (U.S. Patent 4,917,450).

Regarding claims 1-3 and 7, Pocholle et al. disclose (see Figure 2) a semiconductor device, comprising: a plurality of processing elements (CPU1-8); and a switcher (RAM) which connects the processing elements to each other, wherein each of the processing elements includes a network interface (see Figure 1; light emitting element and light receiving element) and is connected to the switcher via the network interface. Pocholle et al. further disclose (see Figure 2) the processing elements are located around the switcher (RAM) and the switcher is located at the center position of the semiconductor device. Pocholle et al. also disclose (see Figure 2) each of the processing elements has a function of the same hierarchical level (same processing function for each CPU).

Regarding claim 8, Pocholle et al. further disclose (see Figure 2) at least one of the processing elements (CPU1-8) and the switcher (RAM) are located in a space where light is confined (under 25), and each of the processing elements and the switcher has a light emitting element and a light receiving element (see column 3, lines 3-9), thereby an optical communication is performed between the processing elements and the switcher.

6. Claims 1-5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Levi et al. (U.S. Patent 5,148,504).

Regarding claims 1-5 and 7, Levi et al. disclose (see Figure 10) a semiconductor device, comprising: a plurality of processing elements (102, 103); and a switcher (108) which connects the processing elements to each other, wherein each of the processing elements includes a network interface (109, 110) and is connected to the switcher via the network interface. Levi et al. further disclose (see Figure 10) the processing elements are located around the switcher (108) and the switcher is located at the center position of the semiconductor device. In addition, Levi et al. disclose (see Figure 10) the processing elements and the switcher are implemented in a single semiconductor chip (common substrate 101) or package. Levi et al. also disclose (see Figure 2) each of the processing elements has a function of the same hierarchical level (both ICs are high performance).

7. Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Carlson et al. (U.S. Patent 5,506,961).

Regarding claims 1 and 6, Carlson et al. disclose (see Figures 1-3) a semiconductor device, comprising: a plurality of processing elements (IOPs); and a switcher (105, 110) which connects the processing elements to each other, wherein each of the processing elements includes a network interface (bus interface; see Figure 2) and is connected to the switcher via the network interface. Carlson et al. also disclose (see Figures 1-3 and column 6, lines 10-14) one of the processing elements (server connection manager) and the switcher (112) are connected by peer-to-peer connection via at least one transmission line (bus).

8. Claims 1 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (U.S. Patent 5,506,961).

Regarding claims 1 and 9-12, Yoshimura et al. disclose (see Figure 1) a semiconductor device, comprising: a plurality of processing elements (1a-1d); and a switcher (26a, 26b) which connects the processing elements to each other, wherein each of the processing elements includes a network interface (24) and is connected to the switcher via the network interface. Yoshimura et al. also disclose (see Figure 21) a plurality of semiconductor chips (20) each of which includes the plurality of processing elements and the switcher; and at least one inter-switcher (26c of Figure 1; included in each element 20) which connects the semiconductor chips to each other. Yoshimura et al. further disclose (see Figure 21) the plurality of semiconductor chips (20) and the inter-switcher are implemented two-dimensionally. In addition, Yoshimura et al. disclose (see Figures 1 and 21) the inter-switcher (26c) is located in one of the plurality of semiconductor chips and the semiconductor chips are implemented three-

dimensionally (the chips have a width, depth and height). Further, since the switcher and the inter-switcher switches signals between circuits, Yoshimura et al. implements a circuit switching.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh X. Luu whose telephone number is (703) 305-0539. The examiner can normally be reached on Monday-Friday from 6:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta, can be reached on (703) 308-4852. The fax phone number for the organization where the application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

txl
October 23, 2002

Thanh X. Luu
Patent Examiner